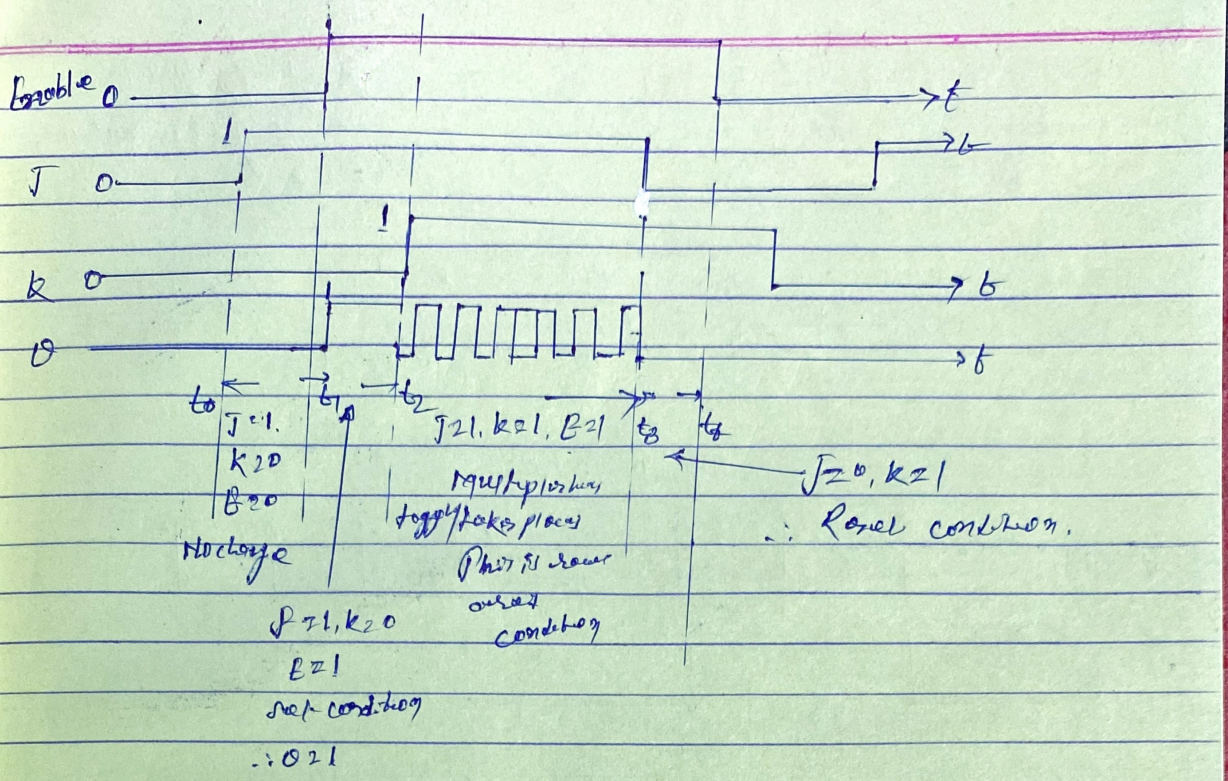


TOGGLE FLIP-FLOP (T-FLIP-FLOP)

Toggle flip-flop is basically a J-K flip-flop with J-K terminals permanently connected together. It is only one input denoted by T. The below figure shows the logic circuit diagram and truth table of T-flip-flop.

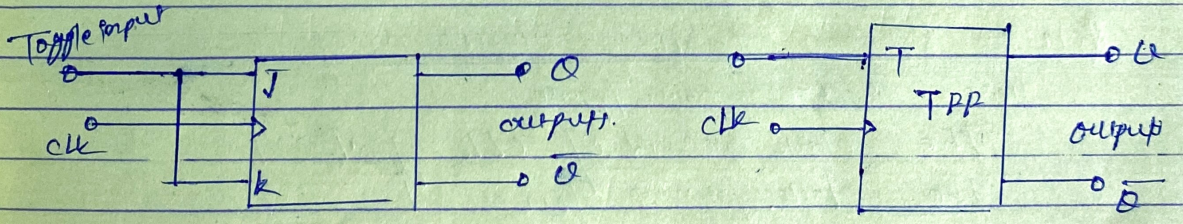


Fig: J-K converted into T-FF

Logic symbol of TFF

Sl. No	clock	Input T	outputs Q_{n+1}	$\bar{Q}_{n+1}$	Comments
1	↑	0	Q_n	$\bar{Q}_n$	NC
2	↑	1	$\bar{Q}_n$	Q_n	Toggle

Q) Determine the current Q for the setup shown in figure 4.40 figure. What is the relation b/w clock freq. and output Q.

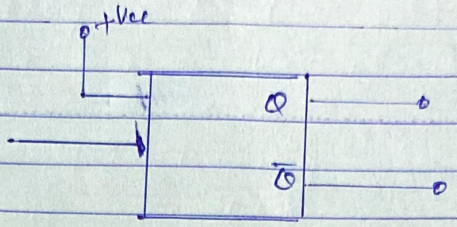
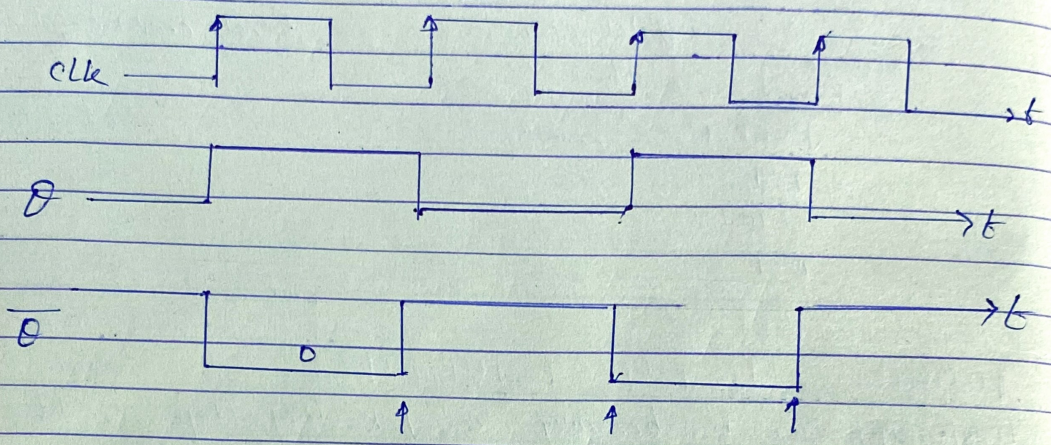


Fig: given figure



Toggling takes place at every leading edge of clock.

Relation between input and output freq.:

Here, from above figure

The clock period of clk signal = T.

The clock freq. $f_{clk} = \frac{1}{T}$

1 cycle period of Q output = 2T

$\therefore$ clock freq. $(f_o) = \frac{1}{2T}$

$\therefore$ Output freq. $(f_o) = \frac{f_{clk}}{2}$

Application of T F/F

It is used as basic building block of a ripple counter.

MASTER SLAVE SR FLIP-FLOP.

A master slave SR flip-flop consists of two edge triggered flip flop, and are connected as shown below.

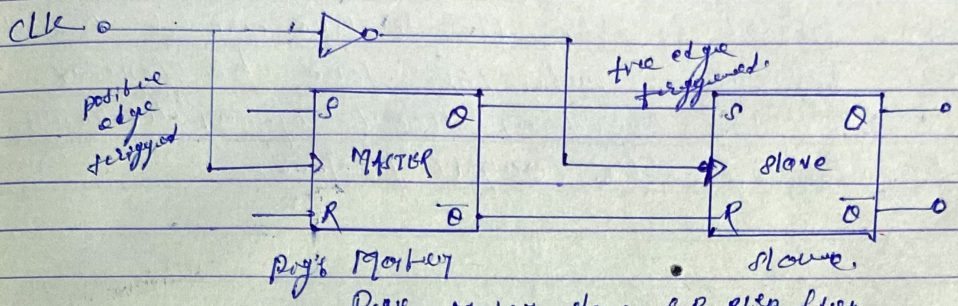
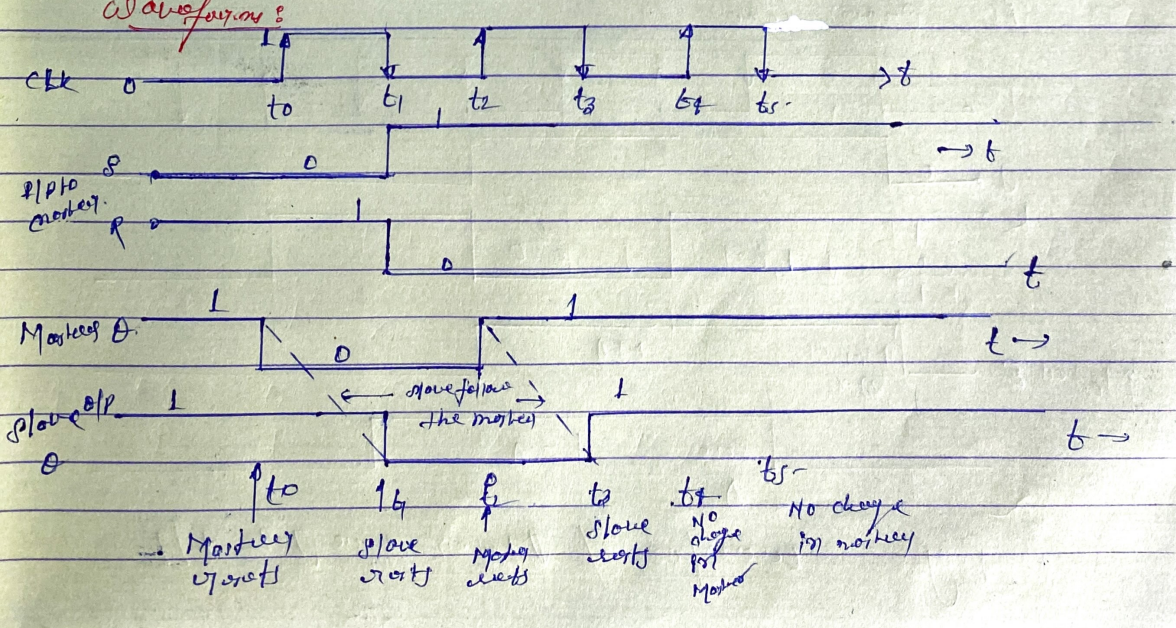


Fig: Master slave S-R flip-flop.

The first flip-flop is called master. It accepts the SR inputs directly. The clock signal is directly applied to directly to the master. The outputs (Q and $\bar{Q}$) of the master are applied to the SR input of slave. The clock signal is inverted and applied to the slave input; that will cause the slave F/F to respond to the low level of the clock.

Waveforms:



Before to, the S and R inputs to the master F/F are S=0, R=1 At t=to CLK=1. This will enable the master and disable the slave. Hence Qout of master becomes low i.e 0. At the same time there is no change for slave output.

At t=t1, The clock signal becomes low(0). This will enable the slave and disable the master. At this instant t1, the I/p to slave are S=0, R=1 Hence slave will reset. This slave has followed the master. In other words Master is transferred to the output of slave.

MASTER SLAVE J-K FLIP-FLOP

The below figure shows the diagram of master J-K flip-flop. The first clocked J-K latch acts as the Master and the other J-K latch acts as slave. The master is positive level triggered and the slave is also the edge triggered. So, when the clock=1 (positive level), the master is active and the slave is inactive. Whereas when clock=0 (low level). The slave is active master is inactive which is shown below.

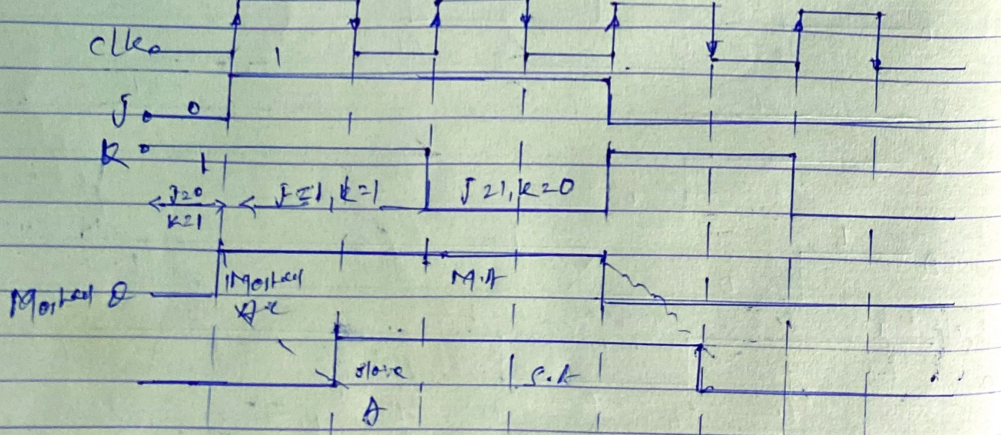
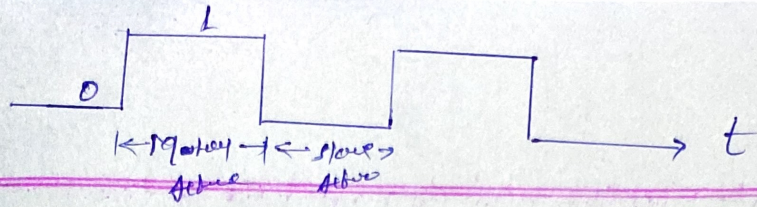


Fig: waveform of Master-Slave J-K F/F



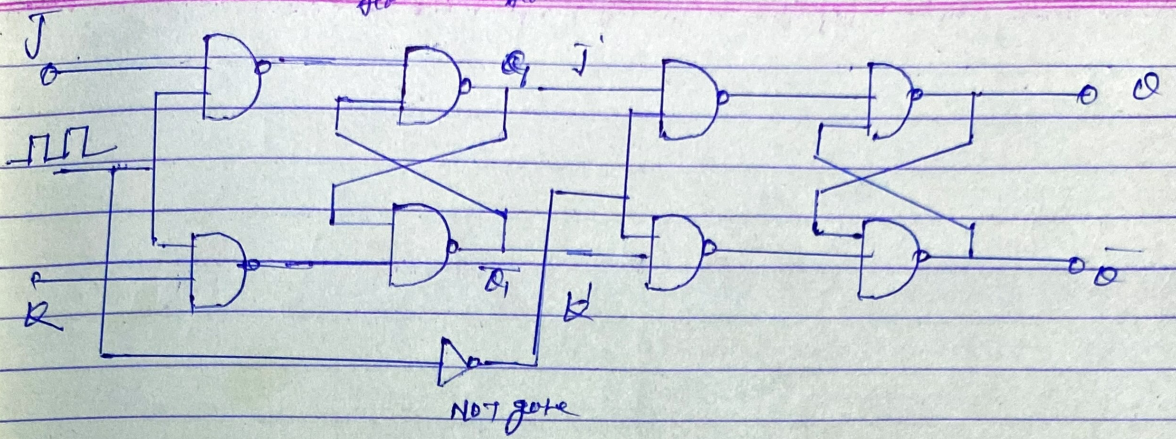


Fig: Master slave J-K flip-flop.